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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/820,374	03/12/1997	Cheol-sung Hwang	SEC.314	2825

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	08/820,374	HWANG, CHEOL-SUNG	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-45* is/are allowed.

6)☒ Claim(s) *25-28 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 1997* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/560,087.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 11/28/06 has been entered.

Response to Arguments

2. Applicant has amended claims 25 and 30 to each further require a step, formed by etching, in the lower substrate. This amendment is supported, by the application as filed, in figure 7 and page 9 lines 1-5 of the specification, which state:

> FIG. 7 shows an etch-back process for controlling the contact layer 19 to a uniform thickness. In the preferred embodiment, ... In the etch-back process of the preferred embodiment, the Pt deposited between the node patterns is preferably overetched, together with a portion of the interlayer insulating film 12 below the Pt layer, so that the nodes are entirely isolated from one another.

It is clear from this description that the same etch (RIE using Ar and Cl_2) is used for overetching third layer 19 and forming the step in interlayer insulating layer 12 (a part of the lower substrate). It is also clear that this overetching step removes at least some of the interlayer insulating film (part 12 in Applicant's figure 7).

Applicant argues that neither Summerfelt et al. 5,566,045 nor Maniar et al. 5,254,217 teach such a step, formed by etching, in the lower substrate. Specifically with respect to Maniar et al. Applicant argues that although Maniar et al. teaches removing, column 6 lines 1-6 and 32-35, all vestiges of the metallic layer (that is patterned to form lower electrode 50) lying over substrate 54, Maniar et al. says not a word about etching substrate 54.

Applicant is correct. Maniar et al. teaches, column 5 lines 27-31, that "it is required that the etching of the first RuO_2 layer proceed to the interface between the first RuO_2 layer and substrate 54 without unduly etching away the surface of substrate 54." Since Maniar et al. also teaches, column 6 lines 32-34, "a substantial over-etch... to remove all portions of the first RuO_2 layer." Maniar et al.'s preferred device is clearly a device in which the substrate is not etched at all. It should be noted, however, that to make their preferred device, Maniar et al. must make the etch process come to a sudden screeching stop at the precise instant that the last vestige of first RuO_2 layer is gone, and before any of substrate 54 can be etched. Maniar et al. does not teach how to accomplish said sudden screeching stop in the etch process.

A more realistic view is probably taken by Matsumoto et al. 5,599,424 (published some five years after Maniar et al.), who explain that in all "conventional" methods (i.e. prior art methods, including the prior art (to Matsumoto et al.) method of Maniar et al.) of completely etching off a metal (Pt, Ru, RuO) layer formed on a substrate (SiO_2 insulating layer), the substrate is "substantially etched." Note column 5 lines 55-60 of Matsumoto et al. Note that the improved method of Matsumoto et al. also etches the underlying substrate when completely removing the overlying metal, but not to the same extent as "conventional" methods. Id.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-28 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over SUMMERFELT ET AL. (5,566,045) in view of MANIAR ET AL. (5,254,217) and MATSUMOTO ET AL. (5,599,424).

A. With regard to claims 25-28 the Figure 23 embodiment of Summerfelt et al. discloses a lower electrode of a capacitor in a semiconductor device, comprising a first layer 34 comprising TiN (note Table, column 12), a material that serves as a barrier against the diffusion of impurities from a lower substrate 32; a second layer 66 formed over the first layer 34, the second layer 66 may comprise RuO2 (note the table entry for layer 66), a material that is, by applicants' admission, easy to pattern; and a third layer 68 formed over top and side surfaces of the second layer 66 and side surfaces of the first layer 34, the third layer 68 may comprise Pt (note the table entry for layer 68), a material having, by applicants' admission, low leakage current properties. Summerfelt et al. does not disclose that the lower substrate exposed by the third layer is overetched to form a step in an upper surface of the lower substrate.

However, Maniar et al. discloses a semiconductor device, comprising a lower electrode 50 of capacitor 60 that is overetched in order to clean substrate 54 of any stray conductive material. Note figure 3 and column 6 lines 26-36 of Maniar et al. Therefore, it would have been obvious to a person having skill in the art to overetch the insulating film of Summerfelt et al.'s semiconductor device, as is taught by Maniar et al., in order to clean up the underlying substrate to thus prevent possible short circuits. Matsumoto et al. would have taught and/or suggested[1] to one of skill in the art that an overetch that completely cleaned all metal from the substrate would also likely etch a step in the underlying substrate.

B. With regard to claims 30-34 the Figure 23 embodiment of Summerfelt et al. discloses a semiconductor device, comprising an insulating (note Table, column 10) film 32 formed over a semiconductor (note Table, column 11) substrate 30; a polysilicon (note Table, column 12) conductive plug 52 formed in the insulating film 32; a first layer 34 formed over the conductive plug 52 and the insulating film 32, the first layer 34 comprising TiN (note Table, column 12), a material that serves as a barrier against the diffusion of impurities from the conductive plug 52 and the semiconductor substrate 30; a second layer 66 formed over the first layer 34, the second layer 66 may comprise

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[1] "JUSTICE BREYER: Winslow. You put it all around the room. All right, we've got it all around the room, and I begin to look at it and if I see over that it somehow teaches me to combine these two things, if it says, Breyer, combine this and that, that's a teaching and then it's obvious. Now, maybe it doesn't have the teaching, it just has the suggestion. Maybe it says, we suggest you combine this or that; okay, then it's obvious. But I don't understand, though I've read it about 15 or 20 times now, I just don't understand what is meant by the term 'motivation.'" Oral arguments, U.S. Supreme Court, 11/28/06, No. 04-1350, KSR International Co. v. Teleflex, Inc., et al.

RuO2 (note the table entry for layer 66), a material that is, by applicants' admission, easy to pattern; and a third layer 68 formed over top and side surfaces of the second layer 66 and side surfaces of the first layer 68 may comprise Pt (note the table entry for layer 68), a material having, by applicants' admission, low leakage current properties. Summerfelt et al. does not disclose that the insulating film exposed by the third layer is overetched to form a step in an upper surface of the lower substrate.

However, Maniar et al. discloses a method of making a semiconductor device, comprising laying conductive metal oxide layer 14 over insulating film 12 and then patterning layer 14 into, for instance, a lower electrode, and overetching in order to clean insulating film 12 of any stray conductive material. Note figure 1, column 2 lines 19-59, column 3 lines 20-33, and column 6 lines 26-36 of Maniar et al. Therefore, it would have been obvious to a person having skill in the art to use Maniar et al.'s improved etching method to overetch the insulating film of Summerfelt et al.'s semiconductor device, as is taught by Maniar et al., in order to clean up the underlying layer to thus prevent possible short circuits. Matsumoto et al. would have taught and/or suggested to one of skill in the art that an overetch that completely cleaned all metal from the insulating film would also likely etch a step in the underlying substrate (since the insulating film forms the top surface of the underlying substrate).

Allowable Subject Matter

4. Claims 36-45 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as, inter alia, a third, low leakage current electrode layer disposed on top and side surfaces of a second, easily patterned electrode layer and on exposed side surfaces of a first, barrier electrode layer formed under the second electrode layer, with the second layer not completely covering the first layer but rather exposing said first layer side surfaces, as recited in claims 36 and 45.

Note that the figure 23 embodiment of Summerfelt et al. discloses all the limitations of claims 36 and 40 except that Summerfelt et al.'s second layer does not expose the side surfaces of Summerfelt et al.'s first layer.

Response to (anticipated future) Arguments

5. Applicant may object to the seemingly cavalier fashion in which evidence of a suggestion or teaching of an overetched step is found. However it is clear, from recent rulings (e.g., *In re Kahn*, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006); *Dystar v. C.H. Patrick*, No. 06-1088, (slip op., available at www.fedcir.gov/opinions/06-1088.pdf)) of the Federal Circuit, that endless *Prufrock*[2]-style agonizings over precisely

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[2] "And indeed there will be time... To wonder, 'Do I dare?' and, 'Do I dare?' ... Shall I part my hair behind? Do I dare to eat a peach?" T.S. Eliot, "The Love Song of J. Alfred Prufrock"

what one having skill in the art could have, should have, or would have done are not required to meet the TSM test. See MPEP § 2144.

In the case at hand, Maniar et al. teach overetching without (according to Maniar et al.'s expressed wish, note column 5 lines 27-31) "unduly etching away the surface of substrate 54." Matsumoto et al. teach, on the other hand, that some etching of the substrate will usually occur when one completely scours away the metal overlying said substrate. One having skill in the art would have understood that etching the substrate is O.K., however, as long as (going back to the teachings of Maniar et al.) the substrate was not "unduly" etched.

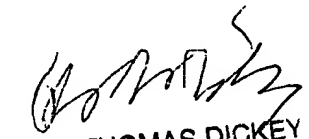
Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



THOMAS DICKEY
PRIMARY PATENT EXAMINER